120 Gbps VCSEL arrays: fabrication and quality aspects

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ABSTRACT
Data centers and supercomputers are driving the demand for short reach aggregate bandwidth. E.g. active CXP active optical cables (AOC) with an aggregate bandwidth of 120 Gbps [1] are being installed since about one year in some of the biggest server farms in the world. As these applications require parallel optics, obviously this is a natural playground for VCSEL technology. The 10G VCSEL platform of Philips ULM Photonics is enabling operation of such AOC at less than 3 W total power by low bias currents for the individual VCSEL as low as 3.4 mA at room temperature and 5.5 mA at 85°C ambient. In combination with ideally matched driver electronics, the launch power of the VCSELs can be stabilized within 0.15dB variation across this operating temperature range [2] and thus allow for open loop power control. With more than 10⁶ hours of operation in the field and no field return reported, the FIT rate for the 1x12 VCSEL array can be calculated to be less than 10 FIT.

Keywords: VCSEL, active optical cable, 10 Gbps, VCSEL arrays

INTRODUCTION
Parallel optics are the natural playing field for VCSEL technology due to the production technique and the low power consumption. In order to meet the demand of very high aggregate bandwidth within supercomputers and datacenters, VCSEL based products have been developped and brought to the market that offer up to 12.5 Gbps per channel and up to 12 channels e.g. in CXP optical cables. The performance aspects of the VCSEL arrays used for these applications are significantly different compared to datacom single channel or QSFP transceivers. As cost efficiency is a major demand for these applications, closed loop power control or fail detection of individual channels is not affordable. Simple temperature compensation and a high quality level have to address these absent features upfront. Obviously, yield of VCSEL arrays plays a dominant role in these cost driven markets. We will present controle features during VCSEL production that allow for high yield, discuss performance aspects on component and module level, using a specific example of combination of Philips Ulm Photonics VCSELs with an Iptronics VCSEL driver, and finally elaborate on quality data including field experience.

DEVICE DESIGN AND PERFORMANCE
Philips Ulm Photonics’ high speed VCSEL platform is based on mesa etching and subsequently laterally oxidized current apertures [3]. For 10 or 12.5 Gbps capable VCSELs, we have chosen a 8.5 µm aperture diameter. For performance of individual dice, homogeneity across VCSEL arrays as well as tight distribution of parameters within the entire population, the control of the mesa diameter, the mesa height, and predominantly the actual aperture diameter is crucial. Highly accurate lithography and hard masking is required for the etching process of the mesa, followed by a well controlled RIE etching step using chlorine based technology. The mesa sidewall is depicted in Fig 1a. In-situ etch depth control allows for an accuracy of the endpoint detection of better than 70 nm [3] and the homogeneity of etching depth across a 3 inch wafer is better than 10%. The sidewall steepness is better than 1 degrees off the targeted 90 degrees, which enables an excellent control of starting conditions for the subsequent lateral oxidation process that defines the current confinement. Taking the benefit of these starting conditions, the oxidation process is controllable to result in a better than +/- 0.5 µm variation across the 3 inch wafer. The chip layout of the 250x250 µm² footprint design is shown in Fig 1b. The dark area is polyimide and the grey area is exposed GaAs.
Resulting LIV characteristics versus temperature for a typical device are depicted in Fig. 2a and Fig. 2b. Threshold current at room temperature is only 0.5 mA and the slope efficiency is designed to 0.35 W/A. At a typical operating current of 6.0 mA, the power variation is 2.0 to 1.0 mW and thus 3dB across the temperature range from –5 to +85°C. The according voltage drop ranges from 1.85 to 1.75 V at 5.0 mA laser current. The series resistance is matched to 50 Ohm.

In order to stabilize the output power across a broad temperature range by temperature compensation schemes, the variation of threshold current and slope efficiency have to be known precisely. In Fig. 3a the parabolic shape of threshold current versus temperature can be seen, showing a minimum threshold current of 0.5 mA at about 35°C. The slope efficiency is linearly decreasing from 0.42 W/A at –5°C down to 0.24 W/A at +85°C, which is computed to 0.5 %/°C.
The already mentioned small variation in active diameters in combination with the excellent homogeneity of the epitaxially grown DBRs, represented by the resonance dip variation of only 3 nm, results in a good homogeneity of device performance across the 3 inch wafers. E.g. threshold current at room temperature varies only between 0.42 mA and 0.60 mA across the wafer, slope efficiency variations are within 0.30 W/A and 0.35 W/A.

In order to secure highest quality level, several measures are taken to ensure performance as well as reliability of the VCSEL arrays. At first, all performance parameters of individual channels are checked against specification. Subsequently, a floating average check is carried out in order to identify individuals that are slightly different in performance compared to neighbors. These individuals are disqualified and named suspicious, although complying to the channel specifications. Finally all channels within one array are checked against homogeneity limits, e.g. slope efficiency of +/- 10% and threshold current of +/- 0.1 mA.

Parasitic capacitance is minimized by only 15 µm oxide width, a rather thick polyimide passivation layer of 3 µm and reduced pad area of 90x90 µm² for wire or flip-chip (stud) bonding. Typical results for small signal response S21 measurement is shown in Fig 5, from which 3 dB modulation bandwidths can be extracted for various laser currents. The modulation bandwidth is in excess of 8 GHz already for laser currents beyond 4 mA. The setup is limiting the measured bandwidth to 10 GHz. In Fig. 6 the 3 dB modulation frequency is plotted against the square root of laser current above threshold. The slope of the resulting graph indicates a modulation current efficiency factor of 4.23 GHz/sqrt(mA).
From S11 parameter measurement, smith charts are created as shown in Fig. 7a, b, and c for laser currents of 4, 6, and 8 mA, respectively. Using a simple equivalent circuit model (see Fig. 8) that takes pad capacitance $C_{pad}$, mirror resistance $R_{mirror}$, active layer capacitance $C_{active}$, and resistance of active layers $R_{active}$ into account, the according values for the discrete elements can be calculated as shown in Table 1.

![Fig. 7a, b, c: Smith diagram for a 10 G VCSEL at laser currents of 4, 6, and 8 mA, respectively.](image)

For a typical operating laser current of 6 mA, the resistance across the active layers ($R_{active}$) is calculated to be 31 Ohms, the DBR resistance is contributing with 18 Ohms, capacitance of the pin-junction and the current confinement structure is 0.86 pF, and finally pad capacitance amounts to 80 fF.

![Fig. 8: Equivalent circuit model.](image)

<table>
<thead>
<tr>
<th>Laser Current [mA]</th>
<th>$R_{active}$ [Ohm]</th>
<th>$R_{mirror}$ [Ohm]</th>
<th>$C_{active}$ [pF]</th>
<th>$C_{pad}$ [fF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>37</td>
<td>18</td>
<td>0.82</td>
<td>80</td>
</tr>
<tr>
<td>4</td>
<td>34</td>
<td>18</td>
<td>0.83</td>
<td>80</td>
</tr>
<tr>
<td>6</td>
<td>31</td>
<td>18</td>
<td>0.86</td>
<td>80</td>
</tr>
<tr>
<td>8</td>
<td>29</td>
<td>18</td>
<td>0.90</td>
<td>80</td>
</tr>
<tr>
<td>10</td>
<td>27</td>
<td>18</td>
<td>0.94</td>
<td>80</td>
</tr>
</tbody>
</table>

![Fig. 6: Modulation current efficiency factor is 4.23 GHz/sqrt(mA).](image)
MODULE PERFORMANCE

In order to check the large signal performance and the module characteristics, an optical link is investigated that consist of a VCSEL driver (IPVD12G011), a VCSEL array from Philips ULM Photonics, a high speed oscilloscope, and a BER measurement setup. The VCSEL driver does provide the option to compensate for the temperature dependent VCSEL power variation. Simple linear scaling of bias current $I_{bias}$ (here maximum current, not average current) and modulation current $I_{mod}$ versus temperature results in a constant average optical output power (AOP) over the broad temperature range of 24 to 85°C. The maximum deviation is as small as –0.15 dB as can seen in Fig 9.

![Temperature compensation scheme for VCSEL output power. Simple linear control of bias and modulation current results in only –0.15 dB maximum deviation of average optical power (AOP).](image)

At temperatures from 24°C to 85°C eye diagrams have been recorded. Over the entire temperature range the eyes are nicely open. The respective settings of maximum driving current $I_{bias}$, modulation current $I_{mod}$, and the resulting average optical power (AOP) are given in the captions of Fig. 10a, b, c, and d, respectively.

![Eye diagrams at different temperatures.](image)
According Bit Error Rate (BER) measurements at room temperature recorded for a link with 300m of multimode fiber are present in Fig. 11. The required received optical power for BER $10^{-14}$ amounts to $-12$ dBm.

Fig. 11: BER measurement using a TIA Eval Board and 300 m of MMF Fiber (CF02B41)

**QUALITY AND RELIABILITY**

In order to meet the very high reliability requirements for the VCSEL arrays Philips ULM Photonics is doing accelerated lifetime testing with VCSELs from each VCSEL wafer subsequent to the 100% on wafer testing. These tests include accelerated high temperature operation life testing (ALT) and temperature humidity bias testing (85°C/85 relative humidity).

Fig. 12a shows the optical power as a function of time for an ensemble of 24 individual VCSELs from one wafer, highly stressed at 170°C substrate temperature and 6mA bias current. Measurement of the optical output power of the devices is done every 24 hours at room temperature. From this measurement, the time to failure of each VCSEL, which corresponds to a 2dB drop in output power can be extracted. In Fig. 12b the time to failure values of the VCSELs are plotted in a cumulative distribution function and are compared to a fitted lognormal distribution with mean time to failure (MTTF) of 1570 hours and a sigma of 0.23. As can be seen from Fig 12a, the VCSELs show only very marginal burn-in drift and also the drift during the useful lifetime phase can be neglected, which is very important for open loop power control. Moreover the low dispersion of the failure distribution function gives low spontaneous failures during a long lifetime period. This is in accordance to the observed low field return rate.

Fig. 12a: The graph on the left hand shows the optical power as a function of time of an ensemble of 24 VCSELs highly stressed at 170°C substrate temperature and 6 mA bias current.

Fig. 12b: Corresponding time to failure plotted in a cumulative distribution function.
Fig. 13 shows MTTF values at different junction temperatures. From this graph an acceleration factor of 0.7eV can be extracted, giving a MTTF of 60.000 hours at 85°C ambient temperature.

![Arrhenius plot for the MTTF of PhilipsULM Photonics’ 10G VCSEL products. MTTF at 85°C ambient temperature is 60.000 hours.](image)

The temporal evolution of the slope efficiency for an ensemble of 30 VCSELs operated at 6 mA, 85°C ambient temperature and 85% relative humidity is shown in Fig. 14. The devices are stable within the specification limits for more than 8,000 hours. This is especially important for array products, which are typically not hermetically packaged.

![Temporal evolution of slope efficiency of 30 devices from a wafer during temperature humidity bias testing at 85°C ambient temperature and 85% relative humidity.](image)

After dicing the wafer into individual 1x12 arrays, 100% of the devices are optically inspected. For this purpose, high resolution pictures are taken to judge bonding pad, emission area, and chip edge quality. Fig. 15 shows a sample picture of one channel from a 1x12 array on dicing tape. The shown VCSEL has a contamination in the emission facet and the array has been inked out after optical inspection.

![Sample picture of one channel from a 1x12 array on dicing tape.](image)
Starting early 2009, CXP products equipped with Ulm Photonics’ VCSEL arrays are installed in server farms worldwide. More than 100 million accumulated hours of operation can be calculated for the installed array products. So far no field return due to VCSEL failure has been reported which can be computed to less than 10 FIT for the 1x12 VCSEL arrays, or less than 1 FIT for an individual channel.

OUTLOOK BEYOND 10 GBPS

In order to scope with the demand for even higher accumulated bandwidth in combination with the target settings of costs per Gbps, higher transmission rate per channel is mandatory. The presented platform is also capable of providing 12.5 Gbps data rates as can be seen from the eye diagram in Fig. 16.

Fig. 15: Sample picture from optical inspection of 1x12 array.

Fig. 16: Eye diagram recorded at 12.5 Gbps using the identical devices as introduced in the paragraphs above.

Even higher data rates up to and beyond 25 Gbps are under development and promising results have already been reported so far from various groups, e.g. [4], [5].

ACKNOWLEDGEMENT

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REFERENCES